	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L3	214	(clean$3 with pressure with torr) same (wafer or semiconductor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/30 15:11			0
2	BRS	L4	135	3 and @pd<=20010427	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/30 15:26			0
3	BRS	L5	13	ambient same (transfer$4 with (substrate or semiconductor) with clean with environment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/30 15:26			0
4	BRS	L6	8	5 and @pd<=20010427	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/30 15:26			0

103a, gate electrode sidewall oxide films 103b, etc) where the silicon film (Si-substrate) is not exposed, and no titanium silicide film is formed in such a region. That is to say, the titanium silicide films 104 are formed in a self-aligned manner only in the region (source, drain, and gate regions) where the silicon film (Si-substrate) is exposed. Then, arsenic ions are doped to a 1.times.10.sup.15 -1.times.10.sup.16 /cm.sup.3 dose at 20 KeV-40 KeV through the ion implantation to form the third impurity diffusion regions 108. Then, after the titanium nitride film and unreacted titanium film are removed using a mixed solution of sulfuric acid and aqueous hydrogen peroxide, a second RTA is performed at 950.degree. C.-1000.degree. C. (herein, 1000.degree. C. for ten seconds) to let the titanium silicide films 104 transform to the ones having a stable stoichiometric TiSi.sub.2 C54 crystal structure, and to activate arsenic ions doped to form the n-type third impurity diffusion regions 108.

Detailed Description Text - DETX (85):

Next, as shown in FIG. 6(i), after the silicon nitride films 311 and 312 are removed, a titanium film 326 of about 30 nm thick is deposited. Herein, a cluster type apparatus (not shown) equipped with an argon sputter **cleaning** chamber and a titanium sputter chamber and having a base **pressure** of 1.times.10.sup.-8 -3.times.10.sup.-8 **torr** is used. To be more specific, the silicon nitride films 311 and 312 are etched by argon-sputtering and the **wafer** is transported in vacuum to the titanium sputter chamber, where titanium is sputter-deposited. The above-structured apparatus can deposit a titanium film without forming a natural oxide film in the interface of an activation region of the Si-substrate and the deposited titanium film.

US-PAT-NO: 5880500

DOCUMENT-IDENTIFIER: US 5880500 A

TITLE: Semiconductor device and process and apparatus of fabricating the same

--------- KWIC ---------

DATE ISSUED - PD (1):
19990309

col 11 line 67 - col 13 line 3

Detailed Description Text - DETX (25):

Next, the steps of forming the titanium silicide films 104 and introducing an impurity that will form the third impurity diffusion regions 108 will be described below. Herein, a cluster type apparatus equipped with an argon sputter **cleaning** chamber and a titanium sputter chamber and having a base **pressure** of 1-3.times.10.sup.-8 **torr** is used. To be more specific, after the n-type first and second impurity diffusion regions 105 and 107 are formed (after the impurities are activated by the thermal annealing using the titanium nitride film as an ion implantation cap), the silicon nitride film is etched by argon sputtering and the **wafer** is transported in vacuum to the titanium sputter chamber, where titanium is sputter-deposited. The above-structured apparatus can deposit a titanium film without forming a natural oxide film in the interface of an activation region of the Si-substrate and the deposited titanium film. Note that pure metal titanium (titanium target purity of 99.9999%) is sputter-deposited herein. Next, silicon is doped through the ion implantation in such a manner that a projection range (Rp) comes in the interface of the titanium nitride film, activation region (source and drain regions), and gate polysilicon. By so doing, silicon and titanium near the interface intermix, which facilitates the initial silicidation reaction. Then, a first RTA (Rapid Thermal Annealing) is performed at 575.degree. C.-700.degree. C. (herein, 675.degree. C.) for about ten seconds in nitrogen atmosphere to form a titanium silicide film having a TiSi.sub.2 C49 crystal structure through a titanium-silicon reaction in the silicon film side (gate polysilicon, and source and drain regions of the Si-substrate side), turning the main surface side of the deposited titanium film into a titanium nitride film. At this point, no silicon is supplied to a region (the field oxide films

US-PAT-NO: 6077353

DOCUMENT-IDENTIFIER: US 6077353 A

TITLE: Pedestal insulator for a pre-clean chamber

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20000620

Brief Summary Text - BSTX (6):

In order to fabricate a complete IC, typically several substrate processing systems are used, with each system performing a particular step or series of steps in the overall fabrication process. The substrates are transferred between the systems at **ambient** conditions. The **ambient environment** is maintained very **clean** to prevent contamination of the **substrates as they are transferred** between systems. The substrates may even be transferred in completely enclosed cassettes in order to further prevent contamination thereof. A problem, however, is that it is not possible to prevent the oxygen in the **ambient** air from forming oxides on the surfaces of the substrates. Because the oxidation of the materials in an IC can seriously alter the electrical properties of the materials, oxidized surfaces are undesirable, and the surface oxides, primarily silicon dioxide and metal oxides, need to be removed or etched from the surfaces of the substrates, in a pre-processing cleaning step, before the substrates are subjected to the primary process of the system such as physical vapor deposition and chemical vapor deposition. Particularly, substrate surface features, such as trenches, contacts or vias into which metal conductors, such as tungsten, aluminum or copper, are to be deposited need to be cleaned in order to assure a very low interface resistance between layers of deposition.